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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,509	06/24/2003	Moinul H. Khan	80107.023US1	8807

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,509	KHAN ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6-11,14,15,19,20,22,23,28 and 30-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-11,14,15,19,20,22,23,28 and 30-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communication filed on November 30, 2005. Claim 30 is amended and claims 1, 6-11, 14-15, 19-20, 22-23, 28 and 30-44 are pending in the application.

2. Applicant's arguments filed on November 30, 2004 have been fully considered but deemed to be moot in view of new ground rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 6-8, 11, 14, 19-20, 22, 32-33, 38 and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of James et al. (USPN: 6,026,472) hereinafter, James, further in view of Chauvel (USPN: 6,779,085).

As per claims 1, 6, 11, 20, 38 and 40, Okada teaches a method comprising locking at least one entry in a translation look-aside buffer (TLB) to make the at least one entry available to a process during at least two active periods of the process (i.e. in the time-critical process) and determining a number of entries to lock, i.e. entries associated with the time-critical process (e.g. see Col. 5, lines 27-35). However, Okada does not teach that the step of determining a number of entries to lock comprises

counting unique page access instances during an active period of the process. James, on the other hand, discloses unique page access counter for counting unique page accesses during an active period of the process, i.e. during an active transaction (e.g. see the abstract and Col. 4, lines 29+). James also teaches that the step of determining a number of entries to lock comprises determining a value of a page usage metric for the process, i.e. determining the page access pattern (e.g. see the abstract and Col. 1, lines 59-62). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the unique page access counter taught by James in Okada's method so a record of memory access patterns is created which can be used to optimize memory and process assignments. Therefore, it is being advantageous.

Neither Okada nor James teaches the further limitation of comparing the value of the page usage metric to values of page usage metrics for other processes. Chauvel, on the other hand, teaches that the value of the page usage metric (i.e. the task-id value included with the memory access request) is compared with (sum of) values of page usage metrics for a plurality of other processes (i.e. the selected translated memory address) to determine if they are identical (e.g. see claim 3 and Col. 2, lines 38-41). In other words, the value of the page usage metric (i.e. the task-id value included with the memory access request) and (sum of) values of page usage metrics for a plurality of other processes (i.e. the selected translated memory address) are considered to determine if they are identical; and if they are identical, the TLB miss is declared. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of

the current invention was made to implement the compare step taught by Chauvel in the method taught by the combination of Okada and James. In doing so, it is determined if they are identical or not and based on that it can be determined which entries to lock.

As per claims 7, 19, 32 and 41, the combination of Okada, James and Chauvel teaches the claimed invention as described above and furthermore, James teaches that the step of determining the value of the page usage metric comprises considering an amount of time the process is active by using the interval timer (e.g. see Col. 2, lines 26-33).

As per claims 8 and 33, the combination of Okada, James and Chauvel teaches the claimed invention as described above and furthermore, Okada teaches that the TLB includes a plurality of entries, the method further comprising determining which of the plurality of entries to lock, i.e. it determines entries to lock, which are a part of program performing a time-critical process (e.g. see Col. 2, lines 53-57).

As per claims 14 and 22, the combination of Okada, James and Chauvel teaches the claimed invention as described above and furthermore, James discloses unique page access counter for counting unique page accesses during an active period of the process, i.e. it determines how fast the process is executing by counting unique page accesses during an active transaction so a record of memory access patterns is created which can be used to optimize memory and process assignments (e.g. see the abstract and Col. 4, lines 29+).

4. Claims 9-10 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada, in view of James, further in view of Chauvel.

As per claims 9-10, 34 and 35, the combination of Okada, James and Chauvel teaches the claimed invention as described above. Many different types of replacement/retirement algorithms, such as least recently used/accessed (LRU), most recently used/accessed (MRU), least frequently/commonly used/accessed (LFU), most frequently/commonly used/accessed (MFU), first-in first-out (FIFO), last-in first-out (LIFO), round robin etc., are well-known and notorious old in the art. The replacement/retirement algorithm is a system dependent feature. Replacing an entry is same as unlocking an entry, i.e. locking an entry is opposite than replacing an entry. Since neither applicant nor specification disclose that changing the type of the locking entry (replacement/retirement) algorithm would change the system functionality or performance, therefore, any type of retirement algorithms can be used for determining which of the plurality of entries to lock. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

5. Claims 15, 23, 31, 36-37, 39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada in view of James, further in view of Chauvel, further in view of Gaither (USPN: 6,223,256).

As per claims 15 and 23, the combination of Okada, James and Chauvel teaches the claimed invention as described above, but failed to disclose that the step of determining the number of TLB entries to lock is based, at least in part, on a priority level of the process. Gaither, however, teaches first and second hierarchical section placement algorithms in which TLB entries get locked based on the priority level of the process (e.g. see Col. 10, lines 29-37). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the feature taught by Gaither in the method taught by the combination of Okada, James and Chauvel so the high priority workloads can use most or all TLB entries to avoid delays.

As per claims 31, 36-37, 39 and 42, the combination of Okada, James and Chauvel teaches the claimed invention as described above, but failed to disclose that determining the value of the page usage metric comprises considering a number of previously locked TLB entries for the process. Gaither, on the other hand, teaches that in the Intel scheme, the total number of locked lines in the TLB must be limited to the total number of entries of the TLB or fewer. If the number of locked lines exceeds the total size of the TLB, a deadlock might occur (e.g. see Col. , lines). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the step of considering a number of previously locked TLB entries for the process as taught by Gaither in the method taught by the combination of Okada, James and Chauvel. In doing so, a deadlock situation is avoided by making sure that the number of locked lines does not exceed the total size of the TLB.

6. Claims 28, 30 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greene (USPN: 2004/0139473) in view of Okada, further in view of James, further in view of Chauvel.

As per claims 28 and 43, Greene teaches an electronic system (i.e. the cable modem termination system 110 in Fig. 1) comprising: an amplifier (263 in Fig. 4A) to amplify communications signals; a processor (part of the controller card, 160 in Fig. 1) coupled to the amplifier; and an SRAM storage medium (170 in Fig. 1) accessible by the processor, the storage medium configured to hold instructions (e.g. see Figs. 1 and 4A). However, Greene failed to teach that the processor including a translation look-aside buffer (TLB) with lockable entries and the processor performing locking at least one TLB entry that corresponds to the process. Okada, on the other hand, teaches a processor (MPU, 10 in Fig. 1) including a translation look-aside buffer (TLB) (20 in Fig. 1) with lockable entries (e.g. see Col. 2, lines 53-57). Furthermore, Okada teaches that the processor performing locking at least one TLB entry that corresponds to the process (i.e. in the time-critical process) and determining a number of entries to lock, i.e. entries associated with the time-critical process (e.g. see Col. 5, lines 27-35). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the TLB with lockable entries and locking at least one TLB entry that corresponds to the process in Greene's system as taught by Okada. In doing so, it considerably improves performance of the system by reducing the number of TLB miss.

Both, Greene and Okada, failed to disclose that the processor performing counting a number of unique page accesses made by a process. James, however, discloses unique page access counter for counting unique page accesses during an active period of the process, i.e. during an active transaction (e.g. see the abstract and Col. 4, lines 29+). James also teaches that the method further comprising determining a value of a page usage metric from the number of unique page accesses, i.e. creating a record of memory access patterns from the results of unique page access counters; and determining the number of TLB entries to lock in response to the value of the page usage metric, i.e. determining the page access pattern (e.g. see the abstract, Col. 1, lines 59-62 and Col. 4, lines 29+). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the unique page access counter taught by James in the system taught by the combination of Greene and Okada so a record of memory access patterns is created which can be used to optimize memory and process assignments. Therefore, it is being advantageous.

None of Greene, Okada and James teaches the further limitation of comparing the value of the page usage metric to values of page usage metrics for other processes. Chauvel, on the other hand, teaches that the value of the page usage metric (i.e. the task-id value included with the memory access request) is compared with (sum of) values of page usage metrics for a plurality of other processes (i.e. the selected translated memory address) to determine if they are identical (e.g. see claim 3 and Col. 2, lines 38-41). In other words, the value of the page usage metric (i.e. the task-id value

included with the memory access request) and (sum of) values of page usage metrics for a plurality of other processes (i.e. the selected translated memory address) are considered to determine if they are identical; and if they are identical, the TLB miss is declared. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the compare step taught by Chauvel in the method taught by the combination of Greene, Okada and James. In doing so, it is determined if they are identical or not and based on that it can be determined which entries to lock.

As per claim 30, the combination of Greene, Okada, James and Chauvel teaches the claimed invention as described above and furthermore, James discloses unique page access counter for counting unique page accesses during an active period of the process, i.e. it determines how fast the process is executing by counting unique page accesses during an active transaction so a record of memory access patterns is created which can be used to optimize memory and process assignments (e.g. see the abstract and Col. 4, lines 29+).

As per claim 44, the combination of Greene, Okada, James and Chauvel teaches the claimed invention as described above and furthermore, James teaches that the step of determining the value of the page usage metric comprises considering an amount of time the process is active by using the interval timer (e.g. see Col. 2, lines 26-33).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Chauvel et al. (USPN: 2002/0073282) also teach the step of comparing the value of the page usage metric to values of page usage metrics for other processes (e.g. see paragraph [0213] and Fig. 22)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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